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EXAMINER	
TRAN, VINCENT HUY	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/753,032	WILSON, THOMAS J.	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8,12-16 and 20-88* is/are rejected.

7)☒ Claim(s) *5,6,9-11 and 17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the communication filed on 1/06/04

2. Claims 1-88 are pending for examination.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 4/19/04 were considered by the examiner.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 20, 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Hardin et. al. U.S. Patent No. 6,658,043 ("Hardin").

6. As per claim 1, Hardin discloses a clock circuit for a data processing system, the circuit comprising:

a phase locked loop (PLL) [10 fig. 1] to generate a clock signal through phase locking to a reference signal [14 fig. 1];

profile memory [54 fig. 1]to store profile data comprising a plurality of entries; the profile memory capable of being updated while the PLL generating the clock signal [col. 8 lines

15-22 – *Where the RAM device 54 is loaded/updated with predetermined set of number that are associated with a particular desired frequency and deviation*] and

a profile state machine [col. 9 lines 46-65]coupled to the profile memory and the PLL, the profile state machine to read the profile data in sequence from the profile memory and to control the PLL to adjust a frequency of the clock signal according to the profile data read in sequence from the profile memory [col. 7 lines 51-63];

wherein a number of entries of a profile read by the profile state machine in sequence to control the PLL is adjustable [col. 4 lines 61-67].

7. As per claim 2, Hardin discloses the profile memory comprises static random access memory (SRAM) [col. 7 line 35].

8. As per claim 3, Hardin discloses the profile state machine spread spectrum modulates the clock signal according to the plurality of entries [col. 9 lines 49-65].

9. As per claim 4, Hardin discloses a position of the profile in the profile memory, read by the profile state machine in sequence to control the PLL, is adjustable [inherent].

10. As per claim 20, 28, Hardin discloses a machine implemented method to control a frequency of a clock signal generated by a phase locked loop, the method comprising:

obtaining profile address information which specifies a location of a profile stored in profile memory [col. 7 lines 33-39]; and

reading, from the profile memory according to the profile address information, profile data of the profile in sequence to control the PLL [col. 7 lines 51-63; col. 4 lines 61-67].

11. Claim 20, 22-26, 28, 30-33, 35, 37-42, 44-47, 49-54, 59, 61-66, 71-81, 84-86 are rejected under 35 U.S.C. 102(a) as being anticipated by Paist et al. U.S. Patent No. 6,919,744 ("Paist").

12. As per claim 20, 28, Paist discloses a machine implemented method to control a frequency of a clock signal generated by a phase locked loop, the method comprising:

obtaining profile address information which specifies a location of a profile stored in profile memory [col. 3 lines 29-30]; and

reading, from the profile memory according to the profile address information, profile data of the profile in sequence to control the PLL [col. 3 lines 35-47; col. 8 lines 14-18].

13. As per claim 22, Paist discloses the system may include two or more spreading profiles where the system may allow for switching between the two or more spreading profiles; and further, allows for a programmable spreading profile that may be changed on demand for a given application. Therefore inherently, Paist system included a SRAM to store and update the spreading profile.

14. As per claim 23, Paist disclose the clock signal is spread spectrum modulated according to the profile [abs].

15. As per claim 24, Paist inherently teach the address information is obtained form the profile memory.

16. As per claim 25, Paist discloses updating a portion of the profile memory while the PLL generates the clock signal [col. 8 lines 14-21].

17. As per claim 26, Paist discloses slewing the clock signal from a first nominal frequency to a second nominal frequency [col. 6 lines 4-9].

wherein the profile data of the profile is read in sequence to spread spectrum modulate the clock signal when the clock signal in the second nominal frequency [col. 6 lines 17-37].

18. As per claim 35, 47, Paist discloses a machine implemented method to control a frequency of a clock signal generated by a PLL, the method comprising:

dynamically switching from using a first profile stored in profile memory to using a second profile stored in the profile memory for spread spectrum modulation of the clock signal [col. 3 lines 29-30; col. 8 lines 5-17 – *allow for spreading profile to be change on demand*].

19. As per claim 37, Paist discloses loading a plurality of profiles into the profile memory, the plurality of profiles comprising a first profile and the second profile [col. 8 lines 5-7].

20. As per claim 38, Paist discloses the system allows for a programmable spreading profile that may be changed on demand for a giving application. Therefore, it is inherent that Paist system including the replacing of the first profile with a third profile in the profile memory.

21. As per claim 39, inherent.

22. As per claim 40, inherent as discloses by Paist in col. 8 line 15-17.

23. As per claim 41, Paist discloses slewing the clock frequency from the first nominal frequency to a second nominal frequency [col. 6 lines 4-9];

wherein the first profile is used for spread spectrum modulation of the clock signal when the clock signal has the first nominal frequency [inherent].

24. As per claim 42, inherent.

25. As per claim 59, Paist discloses a data processing system , comprising:

a phase locked loop (PLL) to generate a clock signal [abs];

see further discussion in claim 35.

26. As per claim 71, Paist discloses a machine implemented method to control a frequency of a clock signal generated by a phase locked loop [abs], the method comprising:

slewing the clock signal from a first nominal frequency to a second nominal frequency using first profile [triangular spreading profile fig. 4] data stored in profile memory of a clock

circuit, the first nominal frequency being substantially different from the second nominal frequency [col. 6 lines 4-16].

27. As per claim 72, Paist discloses the first profile data is used repeatedly to slew the clock signal from the first nominal frequency to the second nominal frequency [col. 6 lines 17-24].

28. As per claim 73, Paist discloses the clock signal is slewed from the first nominal frequency to the second nominal frequency in a substantially linear variation with respect to time [fig. 4; col. 8 lines 1-2].

29. As per claim 74, Paist does not explicitly teach the spread spectrum modulating the clock signal using the second profile data after the clock signal is slewed to the second nominal frequency. However, this feature is deemed to be inherent to the Paist's system as show in col. 8 lines 5-21 where the system is allow for switching between the two or more spreading profile. The system of Paist would be inefficient if it was not able to switch to a second profile after the clock signal is slewed in order to optimize the performance of the system.

30. As per claim 78, Paist discloses the PLL is an n-phase PLL ; and each entry of the first profile data selects one of n phased output of the PLL [col. 4 lines 1-18].

31. As per claim 79, Paist discloses a machine readable medium containing executable computer program instructions which when executed by a data processing system cause said

system to perform a method to control a frequency of a clock signal generated by a phase locked loop (PLL), the method comprising:

instructing a clock circuit to slew the clock signal from a first nominal frequency to a second nominal frequency using first profile data stored in profile memory of the clock circuit [abs], the first nominal frequency being substantially different from the second nominal frequency [fig. 3].

32. As per claim 80, see discussion in claim 76.

33. As per claim 81, see discussion in claim 77.

34. Claims 35, 41, 47, 53, 59, 65 are rejected under 35 U.S.C. 102(e) as being anticipated by Sha et al. U.S. Patent No. 6,980,581 ("Sha").

35. As per claim 35, 47, Sha discloses a convention machine implemented method to control a frequency of a clock signal generated by a phase looked loop (PLL), the method comprising:

a memory for storing plurality set of codes [profile] for each frequency at which the spread spectrum clock generator will operate. Specifically, Sha discloses, to get the best EMI reduction for a full range of frequency, a multiple set of codes are require in order to effectively perform spread spectrum modulation as the frequency changes [col. 2 lines 9-29; col. 2 lines 30-46].

Therefore, it is inherent that Sha teaches a method for dynamically switching from using a first profile stored in profile memory [ROM 24 fig. 1] to using a second profile stored in the profile memory for spread spectrum modulation of the clock signal.

36. As per claim 41, inherent.

37. As per claim 59, Sha discloses a data processing system , comprising:

a phase locked loop (PLL) to generate a clock signal [fig. 1];

see further discussion in claim 35.

Claim Rejections - 35 USC § 103

38. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

39. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

40. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

41. Claim 7-8, 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardin in view of Paist.

42. As per claim 12, it is noted that the limitation do not substantially differ from claim 1, with the exception of the new limitation reciting "wherein the profile memory is capable of simultaneously storing a plurality of profiles; and wherein the profile state machine is capable of being dynamically instructed to use one of the plurality of profiles to control the PLL." As demonstrated previously, Hardin anticipated the limitation in claim 1.

However, Hard does not explicitly teach the new limitation discuss above.

Paist teaches another method relates to phase-locked loop circuits and more particularly, to controlling a profile of PLL circuit's output frequency spectrum. Specifically, Paist teaches the profile memory [106 fig. 1] is capable of simultaneously storing a plurality of profiles [col. 8 lines 2-7]; and

wherein the profile state machine [col. 3 lines 44-47] is capable of being dynamically instructed to used one of the plurality of profiles to control the PLL [col. 3 lines 2-21].

Therefore, it would have been obvious to one of ordinary skill in the art to have modified the circuit of Hardin with the profile memory that capable of simultaneously storing a plurality of profile; and wherein the profile state machine is capable of being dynamically switching profile to control the PLL as taught by Paist.

The motivation for doing so would have been to get the best EMI reduction for a particular frequency.

43. As per claim 13, see discussion in claim 2.

44. As per claim 14, see discussion in claim 3.

45. As per claim 15, the circuit of Hardin modified by Paist does not explicitly teach the profile memory stores address information for accessing the plurality of profiles at predetermined locations. However, this feature is deemed to be inherent the Hardin/Paist system since the system of Hardin/Paist would not able to access a particular profile if the plurality of profiles was not locate at a predetermined location.

46. As per claim 16, Hardin teaches the clock circuit [14 fig. 11] is disposed on an integrated circuit chip.

47. As per claim 7, see discussion in claim 12.

48. As per claim 8, see discussion in claim 17.

49. Claims 21, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paist as applied to claim 20 above.

50. As per claim 21, The examiner takes Official Notice that these are merely convention technique to monitor the availability of the memory. Paist taught a system where the memory may including two or more spread profiles [col. 8 lines 1-7]. Therefore, one of ordinary skill in the art would be motivate to modify Paist's system with the means to indicate a size of each profile in order to prevent memory overflow.

51. Claims 34, 27, 44-46, 56-58, 68-70, 83, 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paist as applied to claim 20 or 26 or 35, 41 or 47, 53 or 59, 65 or 79 or 83 above.

52. As per claim 44-46, The examiner takes Official Notice that these are merely convention technique for power reduction and system protection.

53. Claims 36, 43, 48, 55, 60, 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sha as applied to claim 35 or 35 and 41 or 47 above, and further in view of Parikh U.S. Patent 7,061,331.

54. As per claim 36, Sha inherently teaches loading a plurality of profiles into the profile memory, the plurality of profiles comprising a first profile, the second profiles and a third profile;

spread spectrum modulating the clock signal at a first nominal frequency using the first profile [fig. 3b];

spread spectrum modulating the clock signal at the second nominal frequency using the third profile [fig. 3a].

Sha teaches a different set of codes (profile) is requires for each frequency at which the spread spectrum clock generator operate in order to obtain the best EMI reduction. However, Sha does not explicitly teach slewing the clock signal from the first nominal frequency to a second nominal frequency using the second profile.

Parikh teaches a method relates to the reduction of EMI radiated from clock signal. Specifically, Parikh teach another profile which is use during the slewing of the clock signal

from the first nominal frequency to a second nominal frequency where the circuit can become unstable during the period of transition[col. 4 lines 34-57; col. 6 lines 32-46].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the convention method disclosed by Sha with the use of another profile as teach by Parikh in order to minimized the amount EMI during the slewing of the clock signal.

55. As per claim 43, see discussion in claim 36.

56. Claims 82, 87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paist as applied to claim 79 or 83 above.

57. As per claim 82, Paist teaches the profile memory further stores second profile data [col. 8 lines 2-7].

Paist does not explicitly teach instructing the clock circuit to spread spectrum modulate the clock signal using the second profile data after the clock signal is slewed to the second nominal frequency.

However, Paist teaches the present system may allow for switching between the two or more spreading profile. Therefore, it would have been obvious to one of ordinary skill in the art to realize by switching the circuit to the second profile after the clock signal is slewed in order to provide system with the best EMI reduction.

Allowable Subject Matter

58. Claims 5-6, 9-11, 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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